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MONOLITHIC 6-18 GHz 3 BIT PHASE SHIFTER

M.J. Schindler, Y. Ayasli*, A.M. Morris, L.K. Hanes**

Raytheon Research Division
131 Spring Street
Lexington, MA 02173

ABSTRACT

A 6-18 GHz 3 bit GaAs MMIC phase shifter is described. It incorporates novel high-pass/low-pass circuit structures, with 0.7 μm gate length MESFETs as switching elements. MESFET off-state capacitances are incorporated as circuit elements, and need not be resonated, thus broadband performance is readily achieved. Each of the 3 bits (45°, 90°, and 180°) has a unique topology, chosen for optimal performance for its specific phase shift. The total FET gate periphery for all 3 bits is 4.9 mm. The 3 bit chip measures only 49 by 87 mils, and is on a 4 mil GaAs substrate.

INTRODUCTION

A broadband phase shifter can be realized by switching between a low-pass and a high-pass filter (1). For GaAs MMIC implementations, MESFETs are the most readily available switching elements. The gates are used as switch control bias terminals. The FET is modelled as a source to drain resistance in the on-state (when the gate voltage is zero). In the off-state (when gate voltage is between pinch-off and breakdown), the FET is modelled as source-drain, gate-source, and gate-drain capacitors. If the gate is terminated by an RF open, these capacitors can be combined into a single capacitance between source and drain (2).

To implement a phase shifter, it is possible to use FETs to switch between separate high-pass and low-pass filters. In such a design the off-state capacitance of the FETs tends to limit the bandwidth of the phase shifter. Another approach is to include the switching FETs within a lumped element circuit. Depending on the states of the FETs, such a circuit behaves as either a high-pass or a low-pass filter. In such a circuit the off-state capacitance of some FETs are actually used as capacitive elements of a lumped filter (3). Since these capacitances are no longer undesired parasitics, broadband performance is more easily achieved.

CIRCUIT STRUCTURES

A phase shifter was designed with three bits: 45°, 90°, and 180°, each with a unique topology. No single topology was found that could provide adequate broadband performance for all the bits.

The topology used in the 45° bit is shown in Fig. 1(a). This circuit uses five FETs. When FETs F1, F2, and F4 are "on" and F3 and F5 are "off", a 3 element T low-pass filter is realized. In this state F5 is used as a capacitive shunt filter element. The capacitance of F3 is an undesirable parasitic. Since F3 can be made quite small, its capacitance can be minimal. Then L1 and L2 become inductive series filter elements.

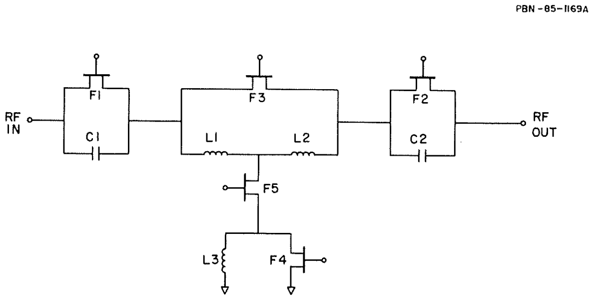

Fig. 1(a) Topology used for the 45° bit.

To realize a 3 element high-pass filter, the biases are reversed. In this state F1 and F2 are used as capacitive series filter elements. Capacitors C1 and C2 are used to increase the capacitance across F1

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* Y. Ayasli is currently with Hittite Microwave, Lexington, MA.

** L.K. Hanes is currently with Raytheon, SMDO, Northboro, MA.

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and F2. The circuit can be made without these capacitors, but then the peripheries of F1 and F2 would become very large, and yield would suffer. The capacitance of F4 is an undesired parasitic which can be minimized. Then L3 becomes an inductive shunt filter element.

The topology of the 90° bit is shown in Fig. 1(b). This is the 3 element T that is used for the 45° bit, with an extra element formed by FET F6 and inductor L4. This bit operates in the same fashion as the 45° bit. In the high-pass state F6 is "on", and L4 becomes an additional inductive shunt filter element. In the low pass state F6 is "off", and since F6 is small, L4 has virtually no effect.

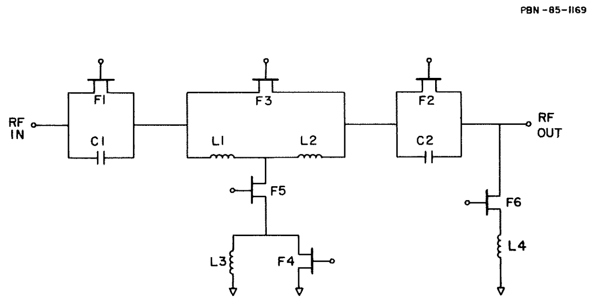

Fig. 1(b) Topology used for the 90° bit.

The 180° bit uses the bridge topology shown in Fig. 1(c) (3). When FETs F1, F2, and F6 are "on" and FETs are F3, F4, and F5 are "off", a 5 element pi high pass filter is realized. When the biases are reversed, a 5 element pi low pass filter is realized. In this circuit the "off" capacitances of some of the FETs are also incorporated as filter elements.

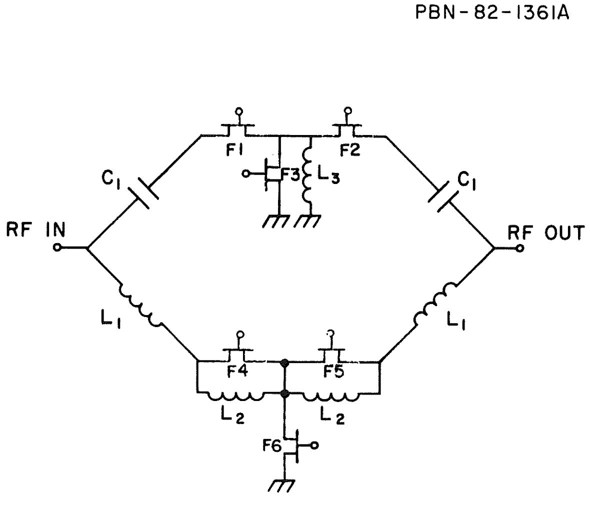

Fig. 1(c) Topology used for the 180° bit.

IMPLEMENTATION

All 3 bits are combined on the MMIC chip is shown in Fig. 2. The 45° bit is on the left side, the 90° bit is on the right side, and the 180° bit is in the center. Appropriate matching networks are used between bits. All the biases are connected to FET gates through 2 kohm resistors. This prevents the bias lines from affecting the RF performance of the FETs, and presents an RF open to the gates. High impedance transmission lines are used as inductors. For large values of inductance the lines are wrapped around to form spirals with less than 2 turns. The minimum line width is 10 μm, and the minimum spacing between lines is 15 μm.

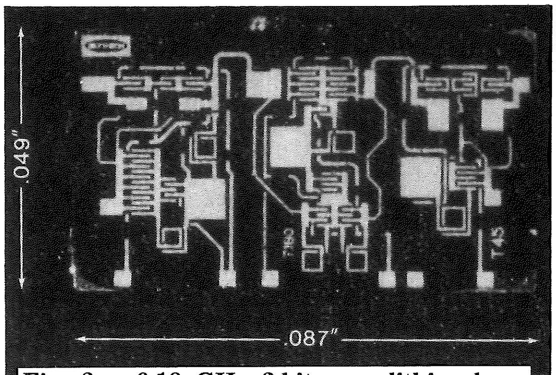

Fig. 2 6-18 GHz 3-bit monolithic phase shifter.

Predicted phase and amplitude responses are shown in Figs. 3 and 4. This type of phase shifter is capable of very good broadband performance.

The circuit was processed on a 4 mil thick, 3 inch diameter GaAs wafer. The MESFETs have 0.7 μm gates written by E-beam. The MESFET active region is doped to $n=10^{17}$ by ion implantation. A highly doped contact layer is use to reduce "on" resistance. The combined MESFET gate periphery for the 3-bit phase shifter is 4.9 mm. The only resistors used are those in the bias circuitry, they have large values (1 kohm and 2 kohm), and are formed by open gate FETs. The capacitors use 5000 angstrom thick silicon nitride as a dielectric. The complete chip measures only 49 by 87 mils.

RESULTS

The measured phase shift of the circuit is indicated in Fig. 5. The accuracy of the phase shift over the 6-18 GHz band is very good. The RMS average phase error over the band is only 8.5°. The RMS phase error in the middle of the band reaches a

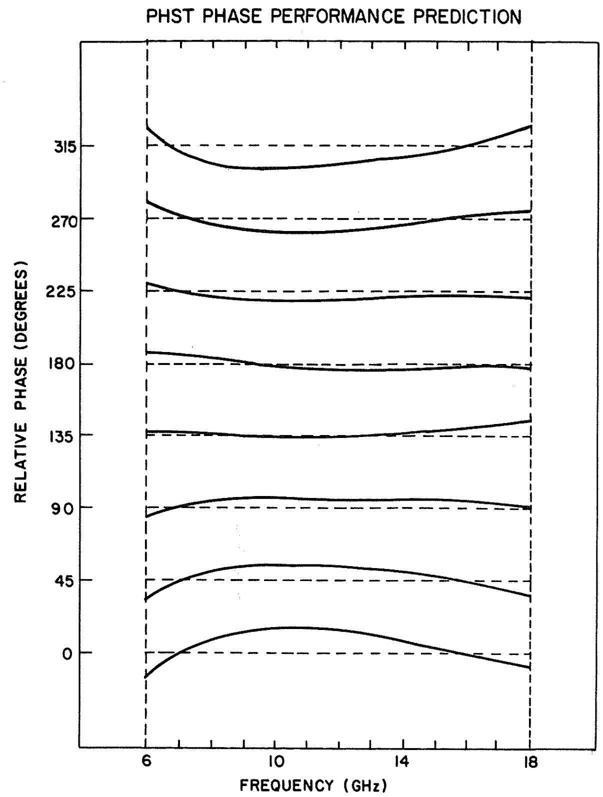

Fig. 3 Predicted phase shifter phase response.

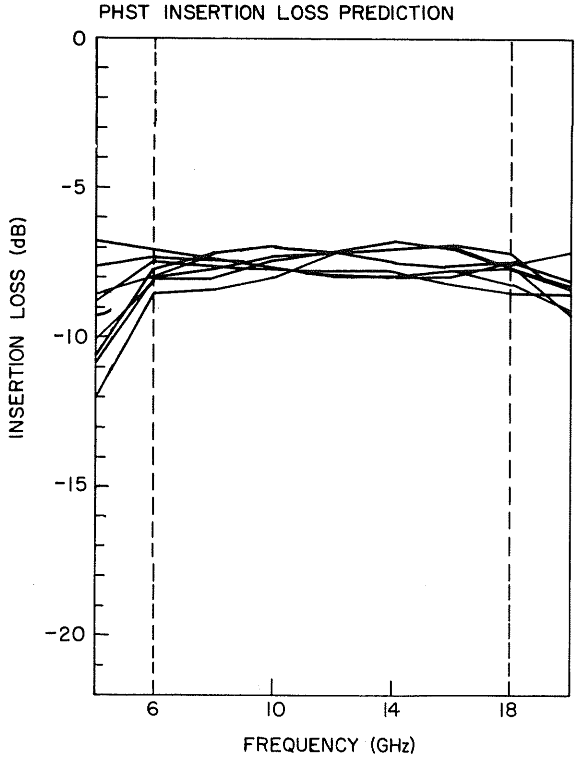

Fig. 4 Measured phase shifter insertion loss.

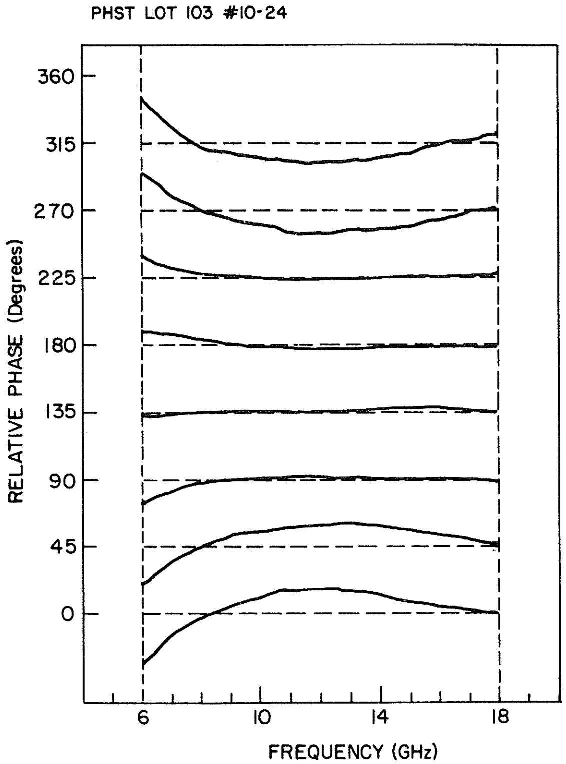

Fig. 5 Measured phase shifter phase performance.

maximum of 10.2°, at the top of the band it is 2.4°. At the bottom band edge the RMS phase error is quite a bit larger than expected, 22.2°. A comparison of predicted and measured performance is tabulated in Table 1.

Table 1
Summary of Predicted and Measured RMS Phase Error

	6 GHz	9 GHz	12 GHz	15 GHz	18 GHz
Predicted	9.4°	7.7°	8.0°	3.2°	7.2°
Measured	22.2°	5.2°	10.2°	6.0°	2.4°

The measured insertion loss is plotted in Fig. 6. The RMS averaged insertion loss over the entire band is 10.4 dB, with a minimum of 8.7 dB at 9 GHz and a maximum of 14.6 dB at 18 GHz. Over most of the band the insertion loss is 2 dB higher than expected, at the top of the band insertion loss is 6 dB higher than expected. The RMS insertion loss variation over all states and across the band is 1.1 dB.

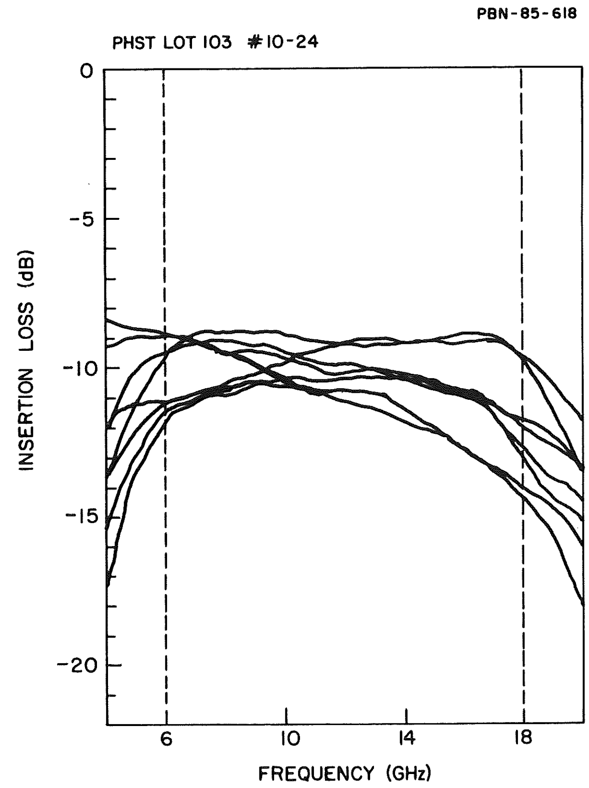

Fig. 6 Measured phase shifter insertion loss.

The measured average return loss is 13 dB. The minimum return loss of 9.0 dB was measured at 18 GHz. This is very much as expected.

The achieved response varies somewhat from the predicted response. The phase error is worse than expected at the bottom of the band, and the insertion loss is worse than expected at the top of the band. These variations can be accounted for by two factors: 1) The actual dielectric thickness of the capacitors is greater than desired; and 2) The model used for the spiral inductors proved inaccurate. It models inductors of up to 2 turns as groups of coupled lines (4). By adding corner effects to the model, a much closer representation of real spiral inductors can be achieved.

CONCLUSION

A 3 bit broadband phase shifter was successfully demonstrated over the 6-18 GHz band. The performance of the phase shifter can be summarized in error power. The total error power is 0.039, not including quantization error. Of this error, 0.017 is contributed by amplitude variations, and 0.022 is contributed by phase variations.

Some new topologies were used in this design. Most of the FETs are used as capacitive filter elements in their "off" states. These "off" state capacitances are not undesired parasitics, so broadband performance is readily achieved. The result is a very small, high performance device, easily produced as a GaAs MMIC.

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